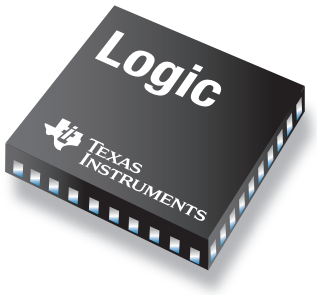


Little Logic Guide

Texas Instruments

Gate Functions

Signal-Switch Functions

Configurable Functions

Translation Functions

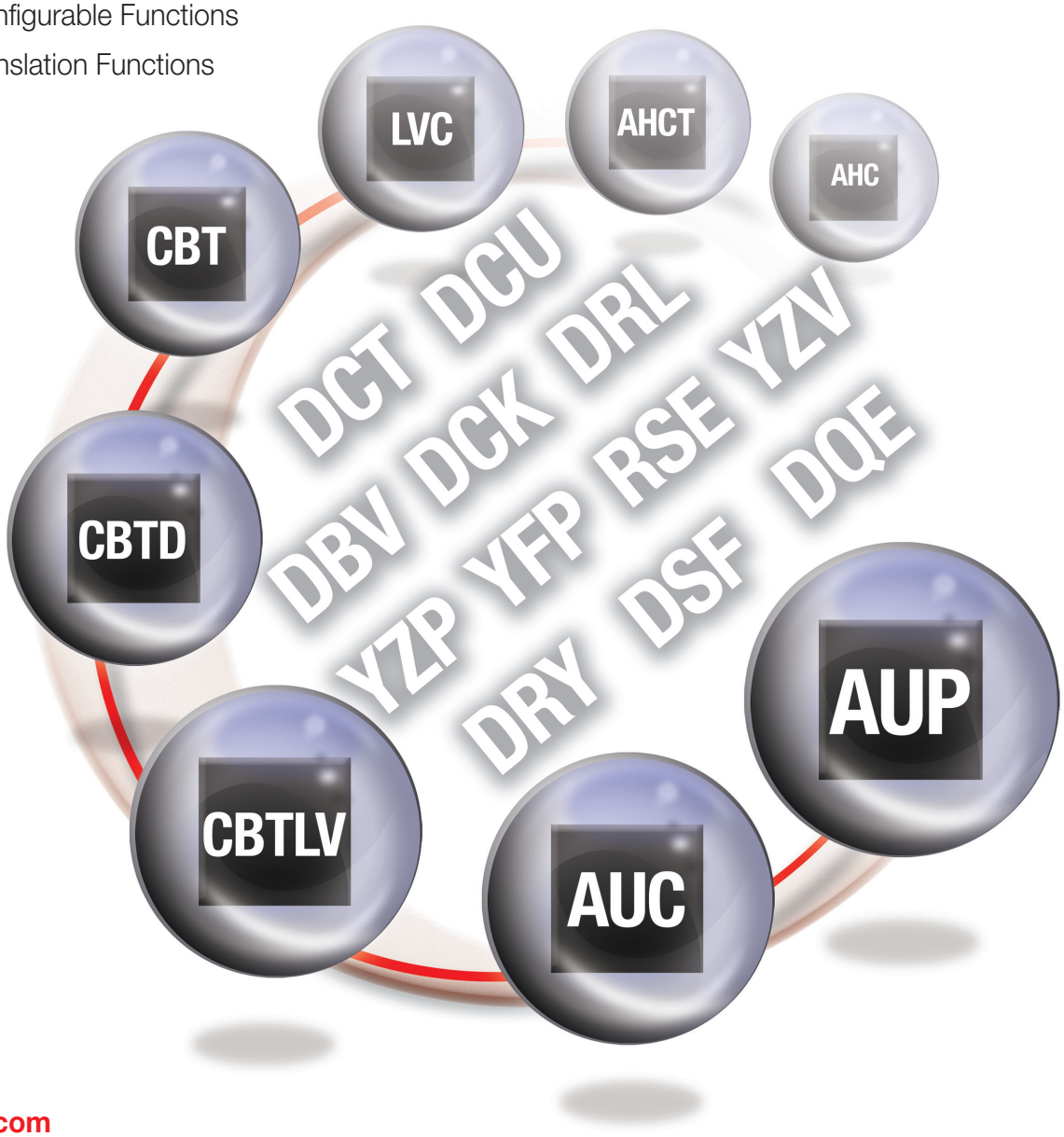


Table of Contents

Overview

A winning design is like a puzzle.
Texas Instruments gives you the right pieces.
Little Logic devices from Texas Instruments (TI) are the pieces that help complete the design puzzle. Their extremely small size gives designers the ability to greatly simplify design routing and maximize ASIC design development.

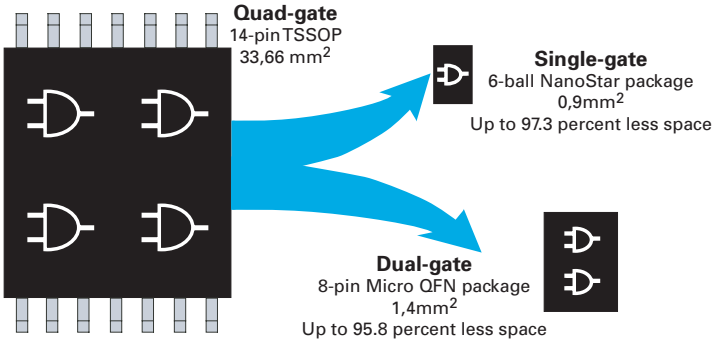
Little Logic devices in 5-/6-pin SOT-23, 5-/6-pin SC-70, 8-pin SSOP, 8-pin VSSOP, 5-pin SOT553, 6-pin SOT563, 6-/8-pin Micro QFN and NanoStar™ integrated circuit packages allow designers to place a particular gate function close to related circuitry, shortening and simplifying routes on a board. This represents a major advance over multiple-gate devices, which require the routing of multiple etches from distinct partitions on a printed circuit board (PCB) through one logic device.

In addition, TI's Little Logic devices also allow designers to alter the output of an ASIC without redesign and manufacture, effectively extending the life of the device and maximizing design investment.

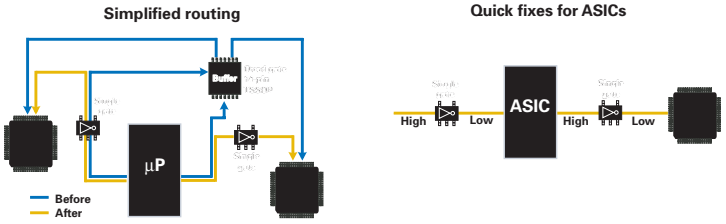
TI's growing line of Little Logic products is helping designers of almost every type of end-equipment build more simple, powerful and cost-effective designs.

If you would like more information on how TI's Little Logic can help you put all of your design pieces together, call your local TI field sales office or your authorized TI distributor, or visit our Web site at www.ti.com/littlelogic.

Space-saving package options



Little Logic technology simplifies board layout and offers better overall performance



Performance Comparisons

Performance Comparisons

Family	Operating voltage range (V)	Optimized voltage (V)	Propagation delay - tpd (typ) (ns)	Output drive (mA)	Input tolerance (V)	I_{OFF} protection
AUP	0.8 to 3.6	3.3	3.5	4	3.6	Yes
AUC	0.8 to 2.7	1.8	2.0	8	3.6	Yes
LVC	1.65 to 5.5	3.3	3.0	24	5.5	Yes
AHC	2.0 to 5.5	5.0	5.0	8	5.5	No
AHCT	4.5 to 5.5	5.0	5.0	8	5.5	No
CBT	4.5 to 5.5	5.0	0.25†	–‡	5.5	Yes
CBTD	4.5 to 5.5	5.0	0.25†	–‡	5.5	Yes
CBTLV	2.3 to 3.6	3.3	0.25†	–‡	3.6	Yes
CB3T	2.5 to 3.6	3.3	0.25†	–‡	5.5	Yes

†The progagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance). The value listed is a maximum.
‡The FET switch has no output drive. The drive current at the output terminal is determined by the drive current of the device connected at the input terminal of the FET switch.

Performance Comparisons

AHC (advanced high-speed CMOS)

- Operating range: 2- to 5.5-V V_{CC}
- 5.0-ns typical t_{pd}

SN74AHC1G00
SN74AHC1G02
SN74AHC1G04
SN74AHC1GU04
SN74AHC1G08
SN74AHC1G14
SN74AHC1G32
SN74AHC1G86
SN74AHC1G125
SN74AHC1G126

AHCT (advanced high-speed CMOS)

- Operating range: 4.5- to 5.5-V VCC
- 5.0-ns typical t_{pd}

SN74AHCT1G00
SN74AHCT1G02
SN74AHCT1G04
SN74AHCT1G08
SN74AHCT1G14
SN74AHCT1G32
SN74AHCT1G86
SN74AHCT1G125
SN74AHCT1G126

AUP (advanced ultra-low-power CMOS)

- Operating range: 0.8- to 3.6-V V_{CC}
- 3.5-ns typical t_{pd}

SN74AUP1G00
SN74AUP1G02
SN74AUP1G04
SN74AUP1G06
SN74AUP1G07
SN74AUP1G08
SN74AUP1G10
SN74AUP1G125
SN74AUP1G126
SN74AUP1G14
SN74AUP1G157
SN74AUP1G17
SN74AUP1G240
SN74AUP1G32
SN74AUP1G332
SN74AUP1G34
SN74AUP1G57
SN74AUP1G58
SN74AUP1G74
SN74AUP1G79
SN74AUP1G80
SN74AUP1G97
SN74AUP1G98
SN74AUP1G99
SN74AUP1T00
SN74AUP1T02
SN74AUP1T04
SN74AUP1T08
SN74AUP1T14
SN74AUP1T157
SN74AUP1T158
SN74AUP1T17
SN74AUP1T32
SN74AUP1T86
SN74AUP1T87
SN74AUP2G00
SN74AUP2G02
SN74AUP2G04
SN74AUP2G06
SN74AUP2G07
SN74AUP2G08
SN74AUP2G125
SN74AUP2G126
SN74AUP2G14
SN74AUP2G17
SN74AUP2G240
SN74AUP2G241
SN74AUP2G32
SN74AUP2G34
SN74AUP2G79
SN74AUP2G80
SN74AUP3G04
SN74AUP3G06
SN74AUP3G07
SN74AUP3G14
SN74AUP3G17
SN74AUP3G34

LVC (low-voltage CMOS)

- Operating range: 1.65- to 5.5-V V_{CC}
- 3.0-ns typical t_{pd}

SN74LVC1G00
SN74LVC1G02
SN74LVC1G04
SN74LVC1GU04
SN74LVC1GX04
SN74LVC1G06
SN74LVC1G07
SN74LVC1G08
SN74LVC1G10
SN74LVC1G11
SN74LVC1G14
SN74LVC1G17
SN74LVC1G18
SN74LVC1G19
SN74LVC1G27
SN74LVC1G29
SN74LVC1G32
SN74LVC1G34
SN74LVC1G38
SN74LVC1G57
SN74LVC1G58
SN74LVC1G66
SN74LVC1G74
SN74LVC1G79
SN74LVC1G80
SN74LVC1G86
SN74LVC1G97
SN74LVC1G98
SN74LVC1G99
SN74LVC1G123
SN74LVC1G125
SN74LVC1G126
SN74LVC1G132
SN74LVC1G139
SN74LVC1G175
SN74LVC1G240
SN74LVC1G332
SN74LVC1G373
SN74LVC1G374
SN74LVC1G386
SN74LVC1G0832
SN74LVC1G3157
SN74LVC1G3208
SN74LVC1T45
SN74LVC2G00
SN74LVC2G02
SN74LVC2G04
SN74LVC2GU04
SN74LVC2G06
SN74LVC2G07
SN74LVC2G08
SN74LVC2G14
SN74LVC2G17
SN74LVC2G32
SN74LVC2G34
SN74LVC2G38
SN74LVC2G53
SN74LVC2G66
SN74LVC2G74
SN74LVC2G79
SN74LVC2G80
SN74LVC2G86
SN74LVC2G125
SN74LVC2G126
SN74LVC2G132
SN74LVC2G157
SN74LVC2G240
SN74LVC2G241
SN74LVC2T45
SN74LVC3G04
SN74LVC3GU04
SN74LVC3G06
SN74LVC3G07
SN74LVC3G14
SN74LVC3G17
SN74LVC3G34

AUC (advanced ultra-low-voltage CMOS)

- Operating range: 0.8- to 2.7-V V_{CC}
- 2.0-ns typical t_{pd}

SN74AUC1G00
SN74AUC1G02
SN74AUC1G04
SN74AUC1GU04
SN74AUC1G06
SN74AUC1G07
SN74AUC1G08
SN74AUC1G14
SN74AUC1G17
SN74AUC1G19
SN74AUC1G32
SN74AUC1G66
SN74AUC1G74
SN74AUC1G79
SN74AUC1G80
SN74AUC1G86
SN74AUC1G125
SN74AUC1G126
SN74AUC1G240
SN74AUC2G00
SN74AUC2G02
SN74AUC2G04
SN74AUC2GU04
SN74AUC2G06
SN74AUC2G07
SN74AUC2G08
SN74AUC2G14
SN74AUC2G17
SN74AUC2G32
SN74AUC2G34
SN74AUC2G53
SN74AUC2G66
SN74AUC2G79
SN74AUC2G80
SN74AUC2G86
SN74AUC2G125
SN74AUC2G126
SN74AUC2G240
SN74AUC2G241
SN74AUC3G04
SN74AUC3GU04
SN74AUC3G06
SN74AUC3G07
SN74AUC3G14
SN74AUC3G17
SN74AUC3G34

Little Logic Signal Switches

CBT (Bus switch)
- Operating range: 4-V to 5.5-V V_{CC}
- 0.25-ns typical t_{pd}

SN74CBT1G125 SN74CBT1G384
SN74CBTD1G125 SN74CBTD1G384

CBTLV (low-voltage bus switch)
- Operating range: 2.3-V to 3.6-V V_{CC}
- 0.25-ns typical t_{pd}

SN74CBTLV1G125

CB3T (low-voltage translation bus switch)
- Operating range: 2.3-V to 3.6-V V_{CC}
- 0.25-ns typical t_{pd}

SN74CB3T1G125

LVC (low-voltage CMOS)
- Operating range: 1.65-V to 5.5-V V_{CC}
- 3.0-ns typical t_{pd}

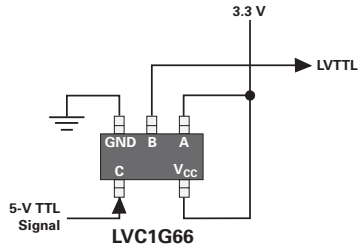
SN74LVC1G66 SN74LVC2G53
SN74LVC1G3157 SN74LVC2G66

AUC (advanced ultra-low-voltage CMOS)
- Operating range: 0.8-V to 2.7-V V_{CC}
- 2.0-ns typical t_{pd}

SN74AUC1G66 SN74AUC2G66
SN74AUC2G53

LVC1G66 TTL-to-LVTTL level shifter

The LVC1G66 can be used for simple translation from 5-V TTL levels to LVTTL. The control pin is tolerant to 5.5 V and, with a maximum ron of 15 W at VCC = 3.3 V, the voltage drop across the switch is only 0.36 V with 24 mA of through current.



Visit **www.ti.com/signalswitches** for the application report, "Selecting the Right TI Signal Switch."

Little Logic Configurables

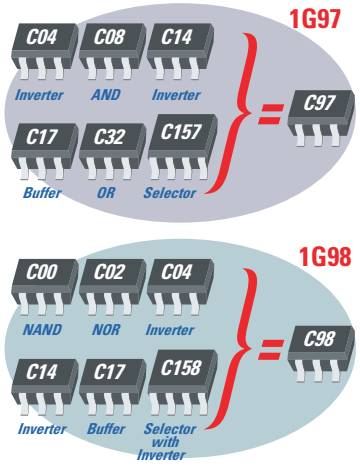
AUP (advanced ultra-low-power CMOS)
- Operating range: 0.8-V to 3.6-V V_{CC}
- 3.5-ns typical t_{pd}

SN74AUP1G57 SN74AUP1G58
SN74AUP1G97 SN74AUP1G98
SN74AUP1G99

LVC (low-voltage CMOS)
- Operating range: 1.8-V to 5.5-V V_{CC}
- 3.0-ns typical t_{pd}

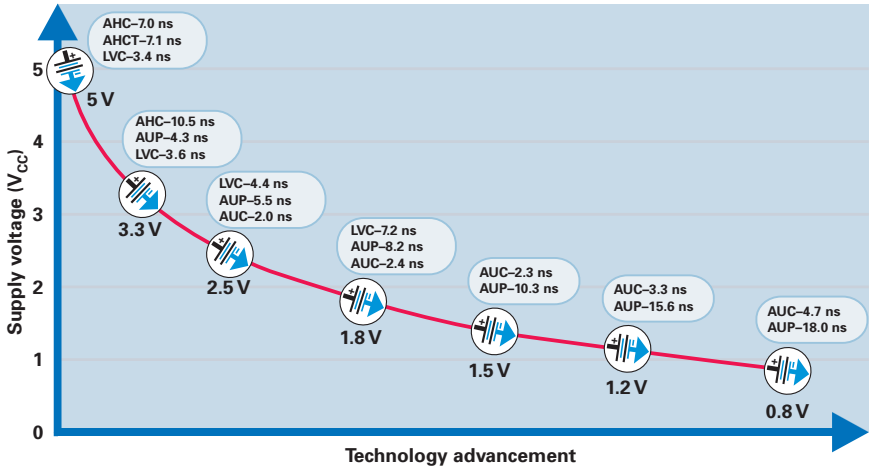
SN74LVC1G57 SN74LVC1G58
SN74LVC1G97 SN74LVC1G98
SN74LVC1G99

The next-generation configurable devices in the Little Logic portfolio are the 1G97/98/99 functions in both the LVC and AUP technologies. By providing nine single-gate logic solutions in the 1G97/98 and 60 functions in the 1G99, the devices allow reductions in device inventory and simplify part management.



Logic Migration to 3.3-V Future

As portable electronics designers look to extend battery life, operating voltages decrease. TI makes the migration to lower operating system voltages simple by offering numerous logic technologies with mixed voltage operation from 5.0-V to 0.8-V. The graph represents TI's logic technology offering in Little Logic at various operating voltages and propagation delays.



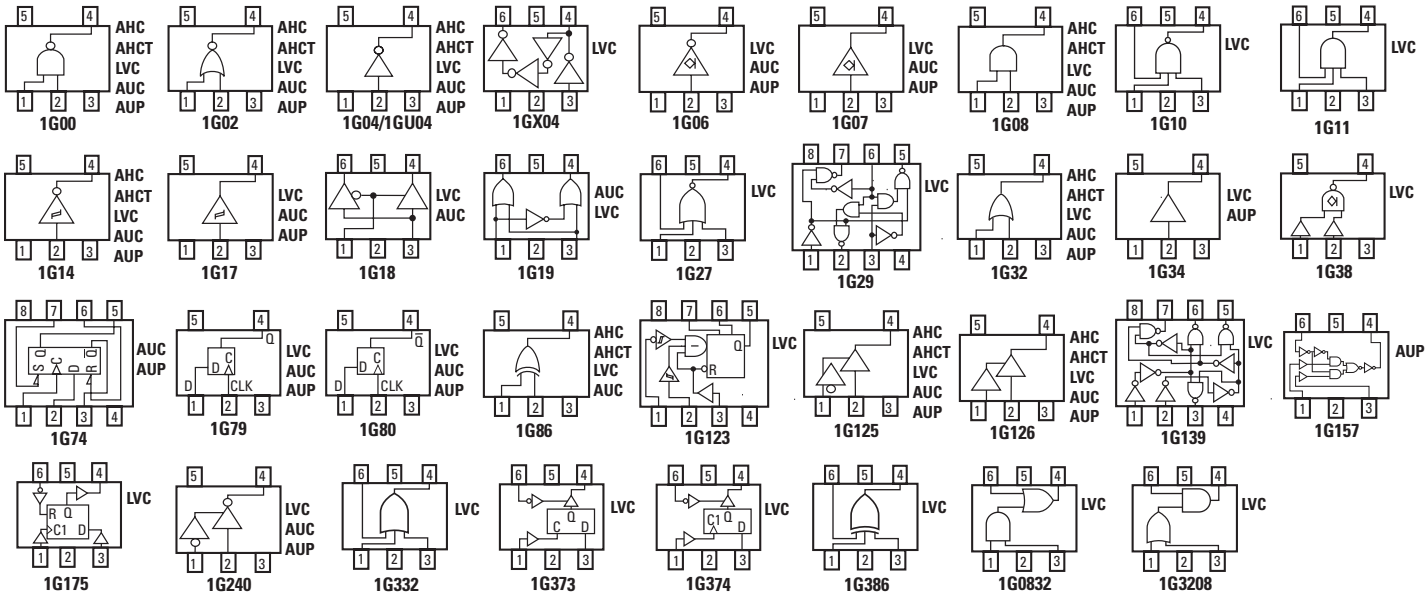
Single-Gate Functions

Single-gate functions

Function	Description	Performance					Package											
		AHC	AHCT	LVC	AUC	AUP	DBV	DCK	DCT	DCU	DQE	DRL	DRY	DSF	RSE	YFP	YZP	YZV
1G00	Single 2-Input NAND Gate	✓	✓	✓	✓	✓	✓	✓				✓	✓	✓		✓	✓	
1G02	Single 2-Input NOR Gate	✓	✓	✓	✓	✓	✓	✓				✓	✓	✓		✓	✓	
1G04	Single Inverter	✓	✓	✓	✓	✓	✓	✓				✓	✓	✓		✓	✓	✓
1GU04	Single Unbuffered Inverter	✓		✓	✓		✓	✓				✓					✓	✓
1GX04	Crystal Oscillator Driver			✓			✓	✓				✓						
1G06	Single Inverter Buffer/Driver w/Open Drain Output			✓	✓	✓	✓	✓				✓	✓	✓		✓	✓	✓
1G07	Single Buffer/Driver w/Open Drain Output			✓	✓	✓	✓	✓				✓	✓	✓		✓	✓	✓
1G08	Single 2-Input AND Gate	✓	✓	✓	✓	✓	✓	✓				✓	✓	✓		✓	✓	
1G10	Single 3-Input NAND Gate			✓		✓	✓	✓					✓	✓		✓	✓	
1G11	Single 3-Input AND Gate			✓			✓	✓									✓	
1G14	Single Schmitt Trigger Inverter	✓	✓	✓	✓	✓	✓	✓				✓	✓	✓		✓	✓	✓
1G17	Single Schmitt Trigger Buffer			✓	✓	✓	✓	✓				✓	✓	✓		✓	✓	✓
1G18	1 of 2 Non-Inverting MUX			✓			✓	✓									✓	
1G19	1 of 2 Decoder/Demultiplexer			✓	✓		✓	✓				✓					✓	
1G27	Single 3-Input NOR Gate			✓			✓	✓									✓	
1G29	2 of 3 Decoder/Demultiplexer			✓					✓	✓							✓	
1G32	Single 2-Input OR Gate	✓	✓	✓	✓	✓	✓	✓				✓	✓	✓		✓	✓	
1G34	Single Buffer Gate			✓		✓	✓	✓				✓	✓	✓		✓	✓	✓
1G38	Single 2-Input NAND Gate w/Open Drain Output			✓			✓	✓						✓			✓	
1G74	Single Positive-Edge-Triggered D-Type Flip-Flop			✓	✓	✓			✓	✓	✓				✓	✓	✓	
1G79	Single D-Type Flip-Flop			✓	✓	✓	✓	✓				✓	✓	✓		✓	✓	
1G80	Single D-Type Flip-Flop			✓	✓	✓	✓	✓					✓	✓		✓	✓	
1G86	Single 2-Input Exclusive-OR Gate	✓	✓	✓	✓		✓	✓				✓					✓	
1G123	Single Retrig Monostable w/Schmitt Trigger Inputs			✓					✓	✓							✓	
1G125	Single Bus Buffer Gate w/3-State Output	✓	✓	✓	✓	✓	✓	✓				✓	✓	✓		✓	✓	
1G126	Single Bus Buffer Gate w/3-State Output	✓	✓	✓	✓	✓	✓	✓				✓	✓	✓		✓	✓	
1G139	2-Line to 4-Line Decoder			✓					✓	✓							✓	
1G157	2-Input Non-Inverting MUX			P		✓		✓					✓	✓		✓		
1G175	Single D-Type Flip-Flop w/Asynch Clr			✓			✓	✓									✓	
1G240	Single Buffer/Driver w/3-State Output			✓	✓	✓	✓	✓					✓	✓		✓	✓	
1G332	Single 3-Input OR Gate			✓		✓	✓	✓				✓	✓	✓		✓	✓	
1G373	Single D-Type Latch w/3-State Output			✓			✓	✓									✓	
1G374	Single D-Type Flip-Flop w/3-State Output			✓			✓	✓									✓	
1G386	Single 3-Input Exclusive-OR Gate			✓			✓	✓									✓	
1G0832	Single 3-Input Positive AND-OR Gate			✓			✓	✓									✓	
1G3208	Single 3-Input Positive OR-AND Gate			✓			✓	✓									✓	

P indicates that this device is Product Preview.
NOTE: Visit www.ti.com/littlelogic for product release updates. Information above valid as of September 2009.

Single-gate diagram



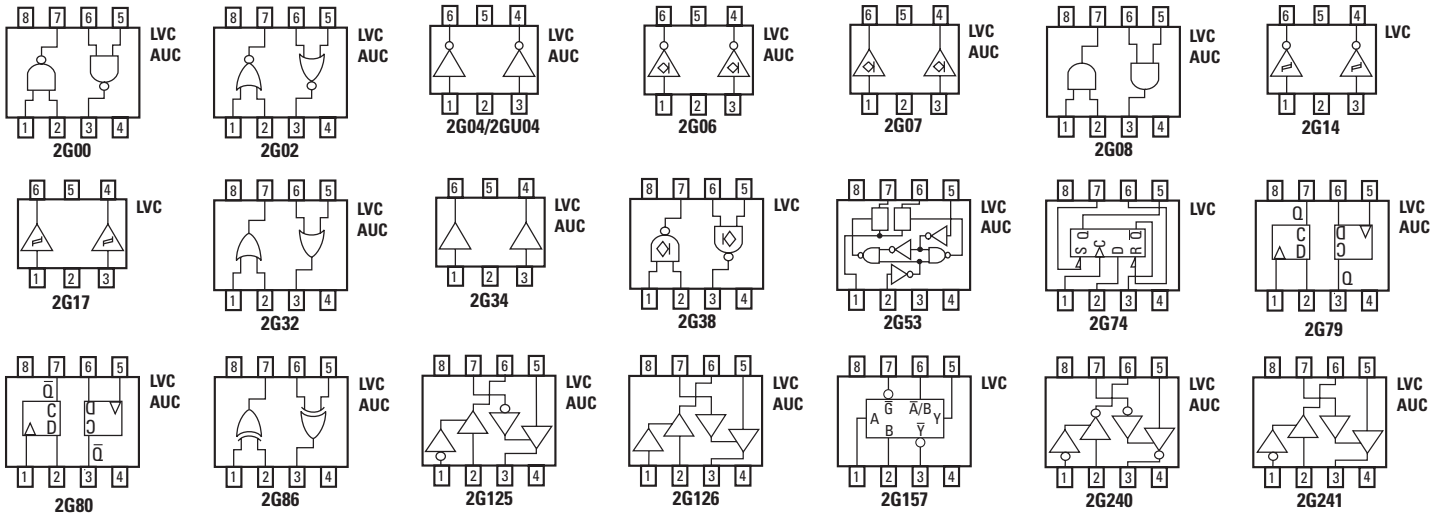
Dual-Gate Functions

Dual-gate functions

Function	Description	Performance			Package										
		LVC	AUC	AUP	DBV (6)	DCK (6)	DCT	DCU	DRL	DRY	DSF	DQE	RSE	YFP	YZP
2G00	Dual 2-Input NAND Gate	✓	✓	✓			✓	✓				✓	✓	✓	✓
2G02	Dual 2-Input NOR Gate	✓	✓	✓			✓	✓				✓	✓	✓	✓
2G04	Dual Inverter	✓	✓	✓	✓	✓			✓	✓	✓			✓	✓
2GU04	Dual Unbuffered Inverter	✓	✓		✓	✓				✓	✓				✓
2G06	Dual Inverter w/Open Drain Output	✓	✓	✓	✓	✓				✓	✓			✓	✓
2G07	Dual Non-Inverter w/Open Drain Output	✓	✓	✓	✓	✓				✓	✓			✓	✓
2G08	Dual 2-Input AND Gate	✓	✓	✓			✓	✓				✓	✓	✓	✓
2G14	Dual Schmitt Inverter	✓		✓	✓	✓				✓	✓			✓	✓
2G17	Dual Schmitt Trigger Input Buffers	✓		✓	✓	✓				✓	✓			✓	✓
2G32	Dual 2-Input OR Gate	✓	✓	✓			✓	✓				✓	✓	✓	✓
2G34	Dual Non-Inverter	✓	✓	✓	✓	✓			✓	✓	✓			✓	✓
2G38	Dual 2-Input NAND Gate w/Open Drain Output	✓					✓	✓							✓
2G53	2:1 Analog Multiplexer/Demultiplexer	✓	✓				✓	✓							✓
2G74	Single Positive-Edge-Triggered D-Type Flip-Flop w/Clear & Reset	✓					✓	✓							✓
2G79	Dual Positive-Edge-Triggered D-Type Flip-Flop	✓	✓	✓			✓	✓				✓	✓	✓	✓
2G80	Dual Positive-Edge-Triggered D-Type Flip-Flop	✓	✓	✓			✓	✓				✓	✓	✓	✓
2G86	Dual 2-Input Exclusive-OR Gate	✓	✓				✓	✓							✓
2G125	Dual Bus Buffer Gate w/3-State Outputs	✓	✓	✓			✓	✓				✓	✓	✓	✓
2G126	Dual Bus Buffer Gate w/3-State Outputs	✓	✓	✓			✓	✓				✓	✓	✓	✓
2G157	Single 2 Line to 1 Line Data Selector/Multiplexer	✓					✓	✓							✓
2G240	Dual Bus Buffer Gate w/3-State Outputs	✓	✓	✓			✓	✓				✓	✓	✓	✓
2G241	Dual Buffer/Driver w/3-State Outputs	✓	✓	✓			✓	✓				✓	✓	✓	✓

NOTE: Visit www.ti.com/littlelogic for product release updates. Information above valid as of September 2009.

Dual-gate diagram



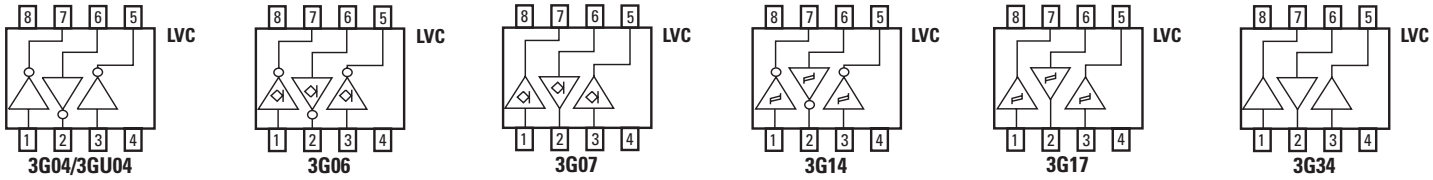
Triple-Gate Functions

Triple-gate functions

Function	Description	Performance		Package					
		AUP	LVC	DCT	DCU	DQE	RSE	YFP	YZP
3G04	Triple Inverter Gate	✓	✓	✓	✓	✓	✓	✓	✓
3GU04	Triple Inverter Gate (Unbuffered)		✓	✓	✓				✓
3G06	Triple Inverter Buffer/Driver w/Open Drain Output	✓	✓	✓	✓	✓	✓	✓	✓
3G07	Triple Buffer/Driver w/Open Drain Output	✓	✓	✓	✓	✓	✓	✓	✓
3G14	Triple Schmitt Trigger Inverter	✓	✓	✓	✓	✓	✓	✓	✓
3G17	Triple Schmitt Trigger Buffer	✓	✓	✓	✓	✓	✓	✓	✓
3G34	Triple Buffer Gate	✓	✓	✓	✓	✓	✓	✓	✓

NOTE: Visit www.ti.com/littlelogic for product release updates. Information above valid as of September 2009.

Triple-gate diagram



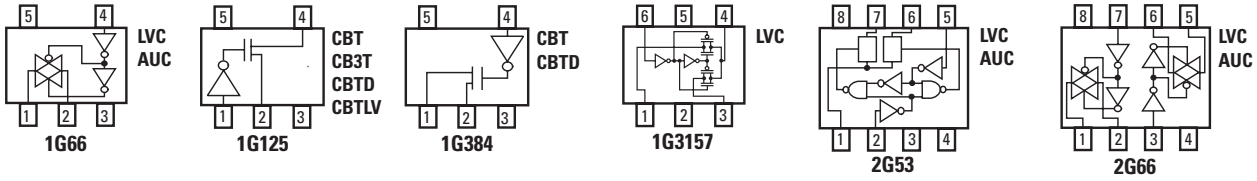
Signal-Switch Functions

Signal-switch functions

Function	Description	Performance						Package							
		CBT	CB3T	CBTD	CBTLV	LVC	AUC	DBV (5)	DCK (5)	DBV (6)	DCK (6)	DCT	DCU	DRL	YZP
1G66	Single Analog Switch					✓	✓	✓	✓					✓	✓
1G125	Single FET Bus Switch	✓	✓	✓	✓	✓	✓	✓	✓					✓	✓
1G384	Single FET Bus Switch	✓		✓				✓	✓						
1G3157	Single-Pole, Double-Throw (SPDT) Analog Switch					✓				✓	✓			✓	✓
2G53	Single-Pole, Double-Throw (SPDT) Analog Switch					✓	✓					✓	✓		✓
2G66	Dual Analog Switch					✓	✓					✓	✓		✓

NOTE: Visit www.ti.com/littlelogic for product release updates. Information above valid as of September 2009.

Signal-switch diagram



Configurable Functions

Configurable functions

Function	Description	Performance		Package								
		LVC	AUP	DBV	DCU	DRL	YZP	YFP	DCK	DRY	DQE	DSF
1G57	Configurable Multiple-Function Gate	✓	✓	✓		✓	✓	✓	✓	✓		✓
1G58	Configurable Multiple-Function Gate	✓	✓	✓		✓	✓	✓	✓	✓		✓
1G97	Configurable Multiple-Function Gate	✓	✓	✓		✓	✓	✓	✓	✓		✓
1G98	Configurable Multiple-Function Gate	✓	✓	✓		✓	✓	✓	✓	✓		✓
1G99	Ultra-Configurable Multiple-Function Gate	✓	✓		✓	✓	✓	✓			✓	

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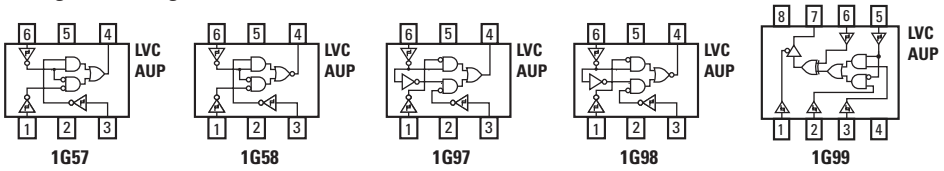
Configurable diagrams



Translation Functions

Translation functions

Function	Description	Performance				Package					
		LVC	AVC	AVCH	AUP	DBV	DCK	DCT	DCU	DRL	YZP
1T00	2-Input NAND Gate				✓		✓				
1T02	2-Input NOR Gate				✓		✓				
1T04	Inverter				✓		✓				
1T08	2-Input AND Gate				✓		✓				
1T14	Schmitt Trigger Inverter				✓		✓				
1T17	Schmitt Trigger Buffer				✓		✓				
1T32	2-Input OR Gate Single-Bit										
1T45	Dual-Supply Transceiver w/Configurable Voltage Translation and 3-State Outputs	✓	✓	✓		✓	✓			✓	✓
2T45	Dual-Bit Dual-Supply Transceiver w/Configurable Voltage Translation and 3-State Outputs	✓	✓	✓				✓	✓		✓
1T57	Single-Supply Voltage-Level Translator with 9 Configurable Gate Logic Functions				✓	✓	✓				✓
1T58	Single-Supply Voltage-Level Translator with 9 Configurable Gate Logic Functions				✓	✓	✓				✓
1T86	2-Input Exclusive-OR Gate				✓		✓				
1T87	2-Input Exclusive NOR Gate				✓		✓				
1T97	Single-Supply Voltage-Level Translator with 9 Configurable Gate Logic Functions				✓		✓				✓
1T98	Single-Supply Voltage-Level Translator with 9 Configurable Gate Logic Functions				✓	✓	✓				✓
1T157	2 to 1 Data Selector/Multiplexer				✓	✓	✓				
1T158	2-Input Multiplexer				✓		✓				

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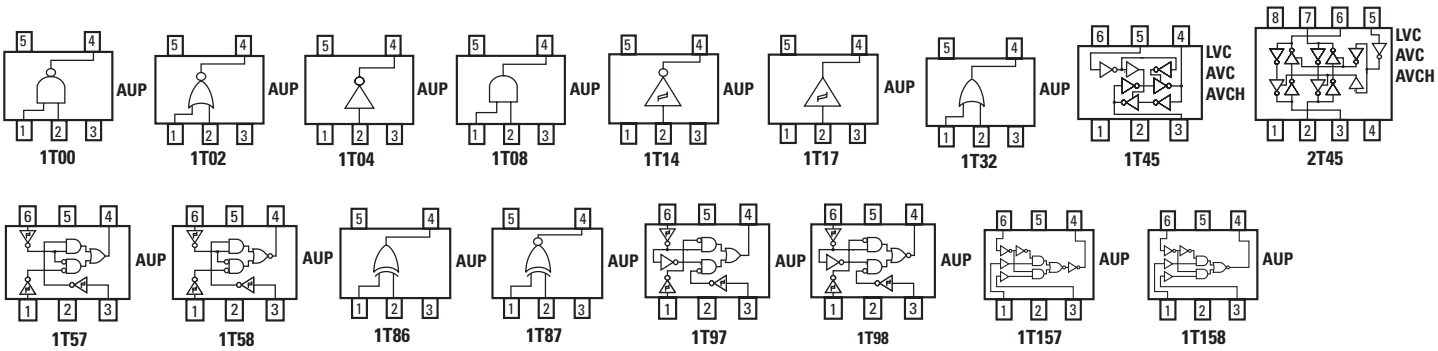
Translation diagrams



AHC devices

Function	Description	TI (AHC)	Toshiba (TC7S/W)	Fairchild (NC7S)	ON (VHC)	STMicro (V1G)	NXP
1G00	Single 2-Input NAND Gate	SN74AHC1G00	TC7SH00	NC7S00	MC74VHC1G00	74V1G00	74AHC1G00
1G02	Single 2-Input NOR	SN74AHC1G02	TC7SH02	NC7S02	MC74VHC1G02	74V1G02	74AHC1G02
1G04	Single Inverter	SN74AHC1G04	TC7SH04	NC7S04	MC74VHC1G04	74V1G04	74AHC1G04
1GU04	Single Inverter (Unbuffered)	SN74AHC1GU04	TC7SHU04	NC7SU04	MC74VHC1GU04	74V1GU04	74AHC1GU04
1G08	Single 2-Input AND	SN74AHC1G08	TC7SH08	NC7S08	MC74VHC1G08	74V1G08	74AHC1G08
1G14	Single Inverter w/Schmitt Trigger	SN74AHC1G14	TC7SH14	NC7S14	MC74VHC1G14	74V1G14	74AHC1G14
1G32	Single 2-Input OR 2	SN74AHC1G32	TC7SH32	NC7S32	MC74VHC1G32	74V1G32	74AHC1G32
1G86	Single 2-Input Exclusive-OR	SN74AHC1G86	TC7SH86	NC7S86	MC74VHC1G86	74V1G86	74AHC1G86
1G125	Single-Bus Buffer Gate w/3-State	SN74AHC1G125	TC7SH125		MC74VHC1G125	74V1G125	74AHC1G125
1G126	Single-Bus Buffer Gate w/3-State	SN74AHC1G126	TC7SH126		MC74VHC1G126	74V1G126	74AHC1G126

AHCT devices

Function	Description	TI (AHCT)	Toshiba (TC7SE/WT)	Fairchild (NC7ST)	ON (VHC1GT)	STMicro (V1T)	NXP
1G00	Single 2-Input NAND	SN74AHCT1G00	TC7SET00	NC7ST0	MC74VHC1GT00	74V1T00	74AHCT1G00
1G022	Single 2-Input NOR	SN74AHCT1G02	TC7SET02	NC7ST02	MC74VHC1GT02	74V1T02	74AHCT1G02
1G04	Single Inverter	SN74AHCT1G04	TC7SET044	NC7ST04	MC74VCH1GT04	74V1T04	74AHCT1G04
1G08	Single 2-Input AND	SN74AHCT1G08	TC7SET08	NC7ST08	MC74VHC1GT08	74V1T08	74AHCT1G08
1G14	Single Inverter w/Schmitt Trigger	SN74AHCT1G14			MC74VHC1GT14	74V1T14	74AHCT1G14
1G32	Single 2-Input OR	SN74AHCT1G32	TC7SET32	NC7ST32	MC74VHC1GT32	74V1T32	74AHCT1G32
1G86	Single 2-Input Exclusive-OR	SN74AHCT1G86	TC7SET86	NC7ST86	MC74VHC1GT86	74V1T86	74AHCT1G86
1G125	Single-Bus Buffer Gate w/3-State	SN74AHCT1G125			MC74VHC1GT125	74V1T125	74AHCT1G125
1G126	Single-Bus Buffer Gate w/3-State	SN74AHTC1G126			MC74VHC1GT126	74V1T126	74AHCT1G126

LVC devices

Function	Description	TI (LVC)	Fairchild (NC7S/WZ)	ON (SZ)	ON (NLU)	ON (NLX)	Toshiba (TC7S/WZ)	NXP (LVC)	Pericom (STX)	STMicro (LX)
Single gate										
1G00	Single 2-Input NAND	SN74LVC1G00	NC7SZ00	NL17SZ00	NLU1G00		TC7SZ00	74LVC1G00		74LX1G00
1G02	Single 2-Input NOR	SN74LVC1G02	NC7SZ02	NL17SZ02			TC7SZ02	74LVC1G02	PI74STX1G02	74LX1G02
1G04	Single Inverter	SN74LVC1G04	NC7SZ04	NL17SZ04	NLU1G04		TC7SZ044	74LVC1G04		74LX1G04
1GU04	Single Inverter (Unbuffered)	SN74LVC1GU04	NC7SZU04	NL17SZU04	NLU1GU04		TC7SZU04	74LVC1GU04	PI74STX1GU04	74LX1GU04
1GX04	Crystal Driver	SN74LVC1GX04						74LVC1GX04		
1G06	Single Inverter Buffer/Driver w/Open Drain	SN74LVC1G06		NL17SZ06				74LVC1G06		
1G07	Single Buffer/Driver w/Open Drain	SN74LVC1G07		NL17SZ07	NLU1G07		TCSZ07	74LVC1G07		74LX1G07
1G08	Single 2-Input AND	SN74LVC1G08	NC7SZ08	NL17SZ08	NLU1G08		TC7SZ08	74LVC1G08	PI74STX1G08	74LX1G08
1G10	Single 3-Input NAND	SN74LVC1G10	NC7SZ10							
1G11	Single 3-Input AND	SN74LVC1G11	NC7SZ11					74LVC1G11		

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LVC devices (continued)

Function	Description	TI (LVC)	Fairchild (NC7S/WZ)	ON (SZ)	ON (NLU)	ON (NLX)	Toshiba (TC7S/WZ)	NXP (LVC)	Pericom (STX)	STMicro (LX)
Single gate										
1G14	Single Inverter w/Schmitt Trigger	SN74LVC1G14	NC7SZ14	NL17SZ14	NLU1G14		TC7SZ14	74LVC1G14		74LX1G14
1G17	Single Buffer w/Schmitt Trigger	SN74LVC1G17		NL17SZ17				74LVC1G17		
1G18	1 of 2 Non-Inverting MUX	SN74LVC1G18	NC7SZ18	NL7SZ18				74LVC1G18		
1G19	1 of 2 Decoder	SN74LVC1G19	NC7SZ19	NL7SZ19				74LVC1G19		
1G27	Single 3-Input NOR	SN74LVC1G27	NC7SZ27							
1G29	2 of 3 Decoder/Demultiplexer	SN74LVC1G29								
1G32	Single 2-Input OR	SN74LVC1G32	NC7SZ32	NL17SZ32	NLU1G32			74LVC1G32		74LX1G32
1G34	Single Buffer Gate	SN74LVC1G34		NL17SZ16			TC7SZ32	74LVC1G34		74LX1G70
1G38	Single 2-Input NAND w/Open Drain	SN74LVC1G38	NC7SZ38				TC7SH34	74LVC1G38		
1G79	Single D-Type Flip-Flop	SN74LVC1G79					TC7SZ38	74LVC1G79		
1G80	Single D-Type Flip-Flop	SN74LVC1G80						74LVC1G80		
1G86	Single 2-Input Exclusive-OR	SN74LVC1G86	NC7SZ86	NL17SZ86	NLU1G86			74LVC1G86		74LX1G86
1G123	Single Retrig Monostable Multivibrator	SN74LVC1G123					TC7SZ86			
1G125	Single-Bus Buffer Gate w/3-State	SN74LVC1G125	NC7SZ125	NL17SZ125				74LVC1G125		74LX1G125
1G126	Single-Bus Buffer Gate w/3-State	SN74LVC1G126	NC7SZ126	NL17SZ126			TC7SZ125	74LVC1G126	PI74STX1G126	74LX1G126
1G132	Single 2-Input NAND w/Schmitt Trigger	SN74LVC1G132					TC7SZ126			74LX1G132
1G139	2-Line to 4-Line Decoder	SN74LVC1G139								
1G175	Single D-Type Flip-Flop w/Asynch Clear	SN74LVC1G175	NC7SZ175					74LVC1G175		
1G240	Single Bus Buffer Gate w/3-State	SN74LVC1G240								
1G332	Single 3-Input OR	SN74LVC1G332	NC7SZ332							
1G373	Single D-Type Latch w/3-State	SN74LVC1G373	NC7SZ373							
1G374	Single D-Type Flip-Flop w/3-State	SN74LVC1G374	NC7SZ374							
1G386	Single 3-Input Exclusive-OR	SN74LVC1G386	NC7SZ386					74LVC1G386		
1G0832	Single 3-Input Positive AND-OR Gate	SN74LVC1G0832								
1G3208	Single 3-Input Positive OR-AND Gate	SN74LVC1G3208								
Dual gate										
2G0	Dual 2-Input NAND	SN74LVC2G00	NC7WZ00	NL27WZ00			TC7WZ00	74LVC2G00		
2G02	Dual 2-Input NOR	SN74LVC2G02	NC7WZ02	NL27WZ02			TC7WZ02	74LVC2G02		
2G04	Dual Inverter	SN74LVC2G04	NC7WZ04	NL27WZ04	NLU2G04	NLX2G04		74LVC2G04		
2GU04	Dual Inverter (Unbuffered)	SN74LVC2GU04	NC7WZU04	NL27WZU04	NLU2GU04	NLX2GU04		74LVC2GU04		
2G06	Dual Inverter Buffer Driver w/Open Drain	SN74LVC2G06		NL27WZ06	NLU2G06	NLX2G06		74LVC2G06		
2G07	Dual-Buffer Driver w/Open Drain Output	SN74LVC2G07	NC7WZ07	NL27WZ07	NLU2G07	NLX2G07		74LVC2G07		
2G08	Dual 2-Input AND	SN74LVC2G08	NC7WZ08	NL27WZ08		NLX2G08	TC7WZ08	74LVC2G08	PI74STX2G08	
2G14	Dual Inverter w/Schmitt Trigger	SN74LVC2G14	NC7WZ14	NL27WZ14	NLU2G14	NLX2G14		74LVC2G14		
2G17	Dual Buffer w/Schmitt Trigger Input	SN74LVC2G17	NC7WZ17	NL27WZ17	NLU2G17	NLX2G17		74LVC2G17		
2G32	Dual 2-Input OR	SN74LVC2G32	NCWZ32	NL27WZ32			TC7WZ32	74LVC2G32		

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LVC devices (continued)

Function	Description	TI (LVC)	Fairchild (NC7S/WZ)	ON (SZ)	ON (NLU)	ON (NLX)	Toshiba (TC7S/WZ)	NXP (LVC)	Pericom (STX)	STMicro (LX)
Dual gate										
2G34	Dual Buffer Gate	SN74LVC2G34	NC7WZ16	NL27WZ16				74LVC2G34		
2G38	Dual 2-Input NAND w/Open Drain	SN74LVC2G38	NCWZ38				TC7WZ38	74LVC2G38		
2G74	D-Type Flip-Flop w/Pre and CLR	SN74LVC2G74	NC7SZ74	NL17SZ74			TC7WZ74	74LVC2G74		
2G79	Dual D-Type Flip-Flop	SN74LVC2G79								
2G80	Dual D-Type Flip-Flop	SN74LVC2G80								
2G86	Dual 2-Input Exclusive-OR	SN74LVC2G86	NC7WZ86	NL27WZ86		NLX2G86		74LVC2G86		
2G125	Dual-Bus Buffer Gate w/3-State	SN74LVC2G125	NC7WZ125	NL27WZ125				74LVC2G125		
2G126	Dual-Bus Buffer Gate w/3-State	SN74LVC2G126	NC7WZ126	NL27WZ126				74LVC2G126		
2G132	Dual 2-Input NAND w/Schmitt Trigger Input	SN74LVC2G132	NC7WZ132							
2G157	2-Input Non-Inverting Mux	SN74LVC2G157								
2G240	Dual-Bus Buffer Gate w/3-State	SN74LVC2G240	NC7WZ240					74LVC2G240		
2G241	Dual-Bus Buffer Gate w/3-State	SN74LVC2G241	NC7WZ241					74LVC2G241		
Triple gate										
3G04	Triple Inverter	SN74LVC3G04	NC7NZ04	NL37WZ04			TC7WZ04	74LVC3G04		
3GU04	Triple Inverter (Unbuffered)	SN74LVC3GU04	NC7NZU04				TC7WZU04	74LVC3GU04		
3G06	Triple Inverter Buffer/Driver w/Open Drain	SN74LVC3G06		NL37WZ06				74LVC3G06		
3G07	Triple Buffer/Driver w/Open Drain	SN74LVC3G07		NL37WZ07				74LVC3G07		
3G14	Triple Inverter w/Schmitt Trigger	SN74LVC3G14	NC7NZ14	NL37WZ14	NLU3G14	NLX3G14	TC7WZ14	74LVC3G14		
3G17	Triple Buffer w/Schmitt Trigger	SN74LVC3G17	NC7NZ17	NL37WZ17	NLU3G17	NLX3G17		74LVC3G17		
3G34	Triple Buffer	SN74LVC3G34	NC7NZ34	NL37WZ16			TC7WZ34	74LVC3G34		

NOTE: Visit www.ti.com/littlelogic for product release updates. Information above valid as of September 2009.

Competitor Cross-Reference (continued)

AUC devices

Function	Description	TI (AUC)	Fairchild (NC7SV)	ON (SV)	Toshiba	Pericom
Single gate (5-pin, unless noted)						
1G00	Single 2-Input NAND	SN74AUC1G00	NC7SV00	NL17SV00	TC7SA00	
1G02	Single 2-Input NOR	SN74AUC1G02	NC7SV02	NL17SV02		
1G04	Single Inverter	SN74AUC1G04	NC7SV04	NL17SV04	TC7SA04	
1GU04	Single Inverter (Unbuffered)	SN74AUC1GU04	NC7SVU04		TC7SAU04	
1G06	Single Inverter Buffer/Driver w/Open Drain	SN74AUC1G06				
1G07	Single 2-Input AND	SN74AUC1G07				
1G08	Single Buffer/Driver w/Open Drain	SN74AUC1G08	NC7SV08	NL17SV08	TC7SA08	PI74ST1G08
1G14	Single Inverter w/Schmitt Trigger	SN74AUC1G14	NC7SV14			
1G17	Single Buffer w/Schmitt Trigger	SN74AUC1G17	NC7SV17			
1G19	1 of 2 Decoder/Demultiplexer	SN74AUC1G19	NC7SV19		TC7PA19	
1G32	Single 2-Input OR	SN74AUC1G32	NC7SV32	NL17SV32	TC7SA32	PI74ST1G32
1G74	D-Type Flip-Flop w/Pre and CLR	SN74AUC1G74	NC7SV74			
1G79	Single D-Type Flip-Flop	SN74AUC1G79				
1G80	Single D-Type Flip-Flop	SN74AUC1G80				
1G86	Single 2-Input Exclusive-OR	SN74AUC1G86	NC7SV86			PI74ST1G86
1G125	Single-Bus Buffer Gate w/3-State	SN74AUC1G125	NC7SV125			PI74ST1G125
1G126	Single-Bus Buffer Gate w/3-State	SN74AUC1G126	NC7SV126			PI74ST1G126
1G240	Single-Bus Buffer Gate w/3-State	SN74AUC1G240				
Dual gate (8-pin, unless noted)						
2G00	Dual 2-Input NAND	SN74AUC2G00				
2G02	Dual 2-Input NOR	SN74AUC2G02				
2G04	Dual Inverter	SN74AUC2G04	NC7WV04		TCPA04	
2GU04	Dual Inverter (Unbuffered)	SN74AUC2GU04			TCPAU04	
2G06	Dual Inverter Buffer/Driver w/Open Drain Output	SN74AUC2G06				
2G07	Dual Buffer/Driver w/Open Drain Output	SN74AUC2G07	NC7WV07			
2G08	Dual 2-Input AND	SN74AUC2G08				
2G32	Dual 2-Input OR	SN74AUC2G32				
2G34	Dual Buffer	SN74AUC2G34	NC7WV16		TC7PA34	
2G79	Dual D-Type Flip-Flop	SN74AUC2G79				
2G80	Dual D-Type Flip-Flop	SN74AUC2G80				
2G86	Dual 2-Input Exclusive-OR	SN74AUC2G86				
2G125	Dual-Bus Buffer Gate w/3-State	SN74AUC2G125	NC7WV125			
2G126	Dual-Bus Buffer Gate w/3-State	SN74AUC2G126				
2G240	Dual-Bus Buffer Gate w/3-State	SN74AUC2G240				
2G241	Dual-Bus Buffer Gate w/3-State	SN74AUC2G241				

NOTE: Visit www.ti.com/littlelogic for product release updates. Information above valid as of September 2009.

Competitor Cross-Reference (continued)

Signal-switch devices

Function	Description	TI	Toshiba	Fairchild	NXP	Pericom
CBT1G125	Single FET Bus Switch	SN74CBT1G125				
CBTD1G125	Single FET Bus Switch	SN74CBTD1G125				
CBT1G384	Single Low-Power Bus Switch	SN74CBT1G384	TC7SB384	NC7SZ384	74LVC1G384	
CBTD1G384	384 Function w/Level Shifting	SN74CBTD1G384	TC7SBD384	NC7SZD384		
CBTLV1G125	Single LV FET Bus Switch	SN74CBTLV1G125				
AUC1G66	Single Analog Switch	SN74AUC1G66				
AUC2G53	SPDT Analog Switch	SN74AUC2G53	TC7PA53			
AUC2G66	Dual Analog Switch	SN74AUC2G66				
LVC1G66	Single Analog Switch	SN74LVC1G66		NC7SZ66	74LVC1G66	
LVC1G3157	SPDT Analog Switch	SN74LVC1G3157		NC7SB3157	74LVC1G3157	PISA3157
LVC2G53	SPDT Analog Switch	SN74LVC2G53				
LVC2G66	Dual Analog Switch	SN74LVC2G66		NC7WB66	74LVC2G66	

AUP devices (5-pin, unless noted)

Function	Description	TI (AUP)	NXP (AUP)	Fairchild (NC7SV)	Toshiba
1G00	Single 2-Input NAND	SN74AUP1G00	74AUP1G00	NC7SP00	TC7SG00
1G02	Single 2-Input NOR	SN74AUP1G02	74AUP1G02	NC7SP02	TC7SG02
1G04	Single Inverter	SN74AUP1G04	74AUP1G04	NC7SP04	TC7SG04
1G06	Single Inverter Buffer/Driver w/Open Drain	SN74AUP1G06	74AUP1G06		
1G07	Single Buffer/Driver w/Open Drain	SN74AUP1G07			
1G08	Single 2-Input AND	SN74AUP1G08	74AUP1G08	NC7SP08	TC7SG08
1G14	Single Inverter w/Schmitt Trigger	SN74AUP1G14	74AUP1G14	NC7SP14	TC7SG14
1G17	Single Buffer w/Schmitt Trigger	SN74AUP1G17	74AUP1G17	NC7SP17	TC7SG17
1G32	Single 2-Input OR	SN74AUP1G32	74AUP1G32	NC7SP32	TC7SG32
1G34	Single Buffer	SN74AUP1G344	74AUP1G34	NC7SP34	TC7SG34
1G74	Single Positive-Edge-Trigger D-Type Flip-Flop	SN74AUP1G74		NC7SP74	
1G79	Single D-Type Flip-Flop	SN74AUP1G79	74AUP1G79		
1G80	Single D-Type Flip-Flop	SN74AUP1G80			
1G125	Single-Bus Buffer Gate w/3-State	SN74AUP1G125	74AUP1G125	NC7SP125	TC7SG125
1G126	Single-Bus Buffer Gate w/3-State	SN74AUP1G126	74AUP1G126	NC7SP126	TC7SG126
1G157	Single 2-Input Non-Inverting MUX	SN74AUP1G157	74AUP1G157	NC7SP157	
1G240	Single-Bus Buffer Gate w/3-State	SN74AUP1G240			

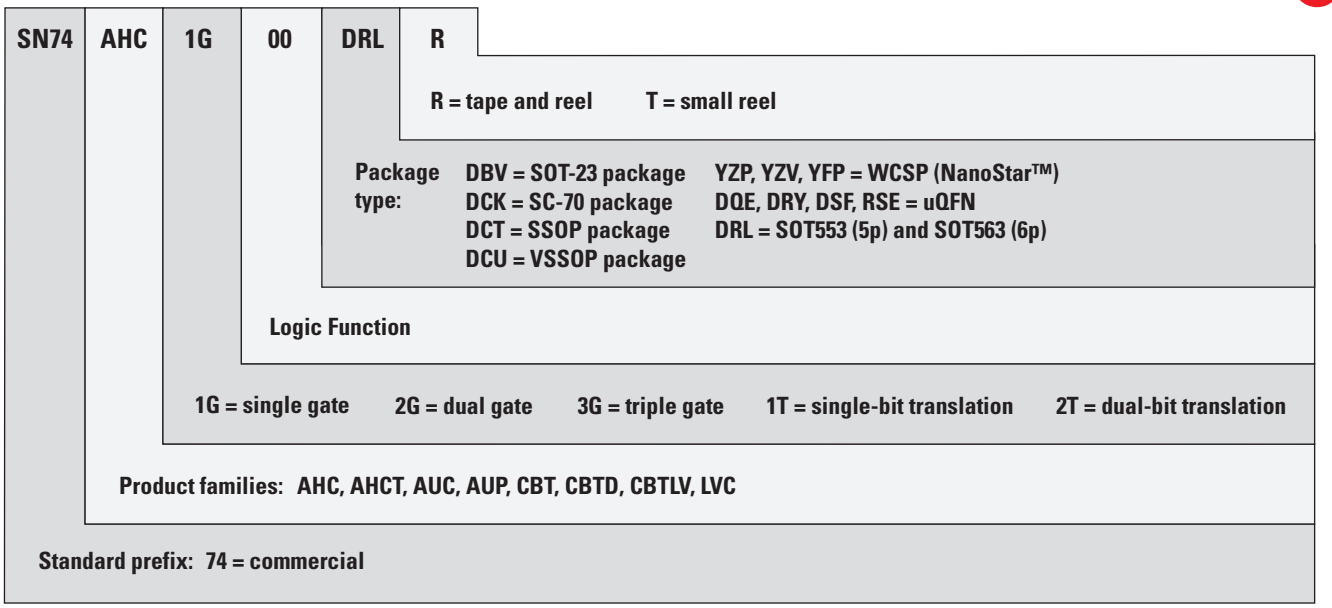
NOTE: Visit www.ti.com/littlelogic for product release updates. Information above valid as of September 2009.

Competitor Cross-Reference (continued)

Configurable devices

Function	Description	TI	Fairchild	NXP
LVC1G57	Single Configurable (5 functions)	SN74LVC1G57	NC7SZ57	74LVC1G57
LVC1G58	Single Configurable (5 functions)	SN74LVC1G58	NC7SZ58	74LVC1G58
LVC1G97	Single Configurable (9 functions)	SN74LVC1G97		
LVC1G98	Single Configurable (9 functions)	SN74LVC1G98		
LVC1G99	Ultra-Configurable (60 functions)	SN74LVC1G99		
AUP1G57	Single Configurable (5 functions)	SN74AUP1G57	NC7SP57	74AUP1G57
AUP1G58	Single Configurable (5 functions)	SN74AUP1G58	NC7SP58	74AUP1G58
AUP1G97	Single Configurable (9 functions)	SN74AUP1G97		
AUP1G98	Single Configurable (9 functions)	SN74AUP1G98		
AUP1G99	Ultra-Configurable (60 functions)	SN74AUP1G99		

Part Number Definition



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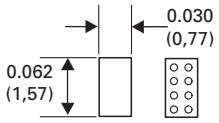
Competitor Part Prefixes

Signal-switch devices

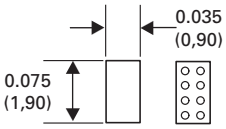
TI	Toshiba	Fairchild	ON	ON (NLU)	ON (NLX)	STMicro	NXP	Pericom
Little Logic								
SN74AHC1G	TC7SH	NC7S	MC74VHC1G			74V1G	74AHC1G	
SN74AHCT1G	TC7SET	NC7ST	MC74VHC1GT			74V1GT	74AHCT1G	
SN74AUC1G	TC7SA/PA	NC7SV	NL17SV					
SN74AUC2G	TC7PA	NC7WV						
SN74AUP1G	TC7SG	NC7SP					74AUP1G	
SN74LVC1G	TC7SZ	NC7SZ	NL17SZ	NLU1G	NLX1G	74LX1G	74LVC1G	PI74STX1G
SN74LVC2G	TC7WZ	NC7WZ	NL27WZ	NLU1G	NLX1G		74LVC2G	PI74STX2G
SN74LVC3G	TC7WZ	NC7NZ	NL37WZ	NLU1G	NLX1G		74LVC3G	
Little Logic signal switches								
SN74AUC2G	TC7PA							
SN74CBT1G	TC7SB	NC7SZ						
SN74CBTD1G	TC7SBD	NC7SZD						
SN74CBTLV1G	TC7SBL							
SN74LVC1G		NC7SZ					74LVC1G	
SN74LVC2G		NC7WB						
Little Logic configurables								
SN74AUP1G		NC7SP						
SN74LVC1G		NC7SZ						
Little Logic translation								
SN74LVC1T		NC7SP						
SN74LVC2T		NC7SZ						

NOTE: Visit www.ti.com/littlelogic for product release updates. Information above valid as of September 2009.

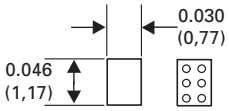
Little Logic Packaging



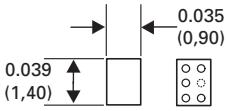
8-Ball WCSP NanoStar™ Package (YFP)
Ball Pitch = 0.016 (0,40)
Height = 0.020 (0,50)
Area = 0.002 (1,29)



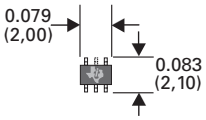
8-Ball WCSP NanoStar Package (YZP)
Ball Pitch = 0.020 (0,50)
Height = 0.020 (0,50)
Area = 0.003 (1,85)



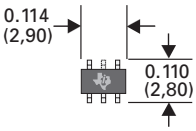
6-Ball WCSP NanoStar Package (YFP)
Ball Pitch = 0.016 (0,40)
Height = 0.020 (0,50)
Area = 0.001 (0,89)



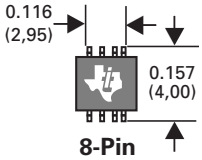
5-/6-Ball WCSP NanoStar Package (YZP)
Ball Pitch = 0.020 (0,50)
Height = 0.020 (0,50)
Area = 0.002 (1,26)



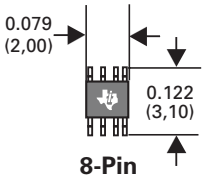
5-/6-Pin SC-70 (DCK)
Lead Pitch = 0.026 (0,65)
Height = 0.037 (0,95)
Area = 0.008 (4.95)



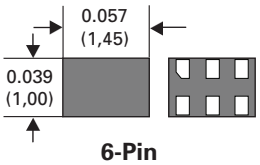
5-/6-Pin SOT-23 (DBV)
Lead Pitch = 0.037 (0,95)
Height = 0.047 (1,20)
Area = 0.014 (9)



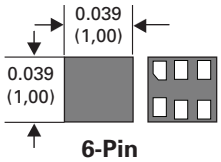
8-Pin SSOP (DCT)
Lead Pitch = 0.026 (0,65)
Height = 0.051 (1,30)
Area = 0.010 (6,72)



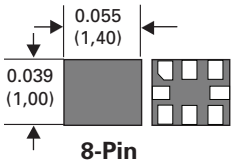
8-Pin VSSOP (DCU)
Lead Pitch = 0.020 (0,50)
Height = 0.035 (0,90)
Area = 0.010 (6,72)



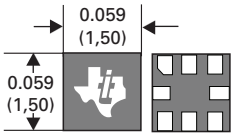
6-Pin Micro QFN (DRY)
Lead Pitch = 0.020 (0,50)
Height = 0.022 (0,55)
Area = 0.002 (1,29)



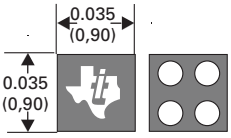
6-Pin Micro QFN (DSF)
Lead Pitch = 0.014 (0,35)
Height = 0.014 (0,37)
Area = 0.001 (0,645)



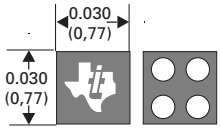
8-Pin Micro QFN (DQE)
Lead Pitch = 0.014 (0,35)
Height = 0.014 (0,37)
Area = 0.002 (1,29)



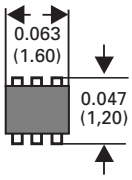
8-Pin Micro QFN (RSE)
Lead Pitch = 0.020 (0,50)
Height = 0.022 (0,55)
Area = 0.003 (1,94)



4-Ball WCSP NanoStar Package (YZV)
Ball Pitch = 0.020 (0,50)
Height = 0.020 (0,50)
Area = 0.001 (0,65)



4-Ball WCSP NanoStar Package (YFP)
Ball Pitch = 0.016 (0,40)
Height = 0.020 (0,50)
Area = 0.009 (0,58)



5-/6-Pin SOT (DRL)
Lead Pitch = 0.020 (0,50)
Height = 0.020 (0,50)
Area = 0.003 (1,94)

Little Logic Package Cross-Reference

Package	TI	Fairchild	ON	Toshiba	NXP	Pericom	STMicro
NanoStar™ Package WCSP	YZP	L6					
SOT-23 (5-pin)	DBV	M5	DT	F	GV	TX	ST
SC-70 (5-pin)	DCK	P5	DF	FU	GW	CX	CT
SOT-23 (6-pin)	DBV	DT			GV		
SC-70 (6-pin)	DCK	P6	DF		DW		
SSOP (8-pin)	DCT			FU			
VSSOP (8-pin)	DCU	K8	US	FK	DC		
SOT563 (6-pin)	DRL		XV5T2	ESV			
NanoStar (4-ball)	YZV						
Micro QFN (8-pin)	DQE						
Micro QFN (8-pin)	RSE	L8	MU		GM		
Micro QFN (6-pin)	DRY	L6	AM		GM		
Micro QFN (6-pin)	DSF	FH	CM		GF		

TI package suffix decoder

YZP is NanoStar package
YZV is NanoStar package

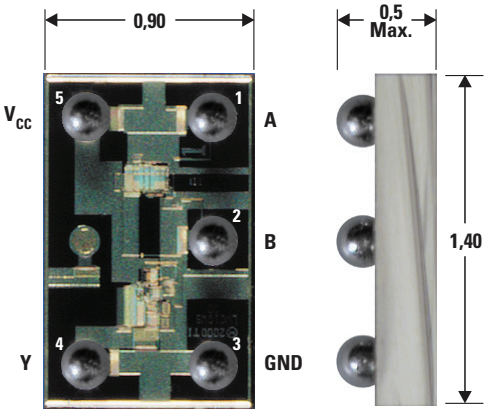
DBV is 5- and 6-pin leadframe
DCK is 5- and 6-pin leadframe, slightly smaller than DBV

DCT is 8-pin leadframe
DCU is 8-pin leadframe, slightly smaller than DCT

DRL is 6-pin plastic small-outline

Introduction to NanoStar Packages

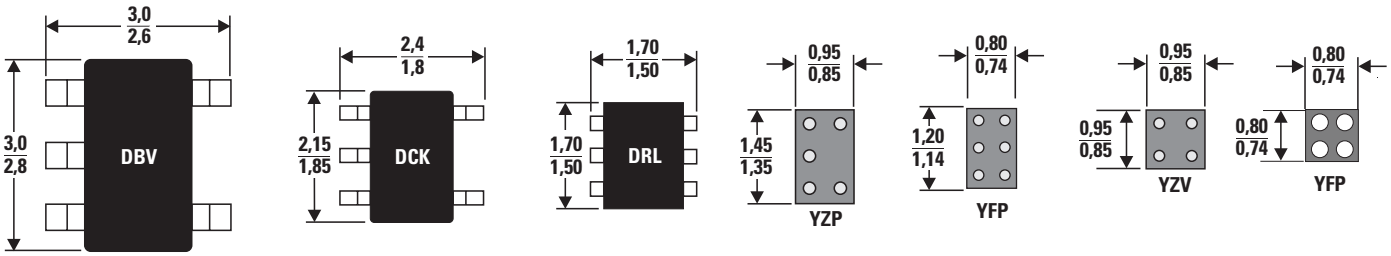
As the marketplace continues to demand size reductions in various consumer electronic products such as cell phones, PDAs, MP3/CD players and other portable devices, the need for smaller logic packaging becomes paramount. The major challenge of today's digital processing industry is overall system cost reduction as complexity and functionality increase. These marketplace forces have resulted in circuit integration and board miniaturization becoming a necessary trend for successful competition. To address these rapidly evolving customer requirements, TI has defined the latest innovation in logic packaging: NanoStar™ packages. This is a wafer-chip-scale package (WCSP) and, to date, is the world's smallest 4-, 5-, 6- and 8-ball logic solution for Little Logic functions.



(Bottom view) Dimensions in millimeters (mm)

Package designator
YZP= Pb-free large ball
YZV= Pb-free large ball

Package Data



Dimensions in millimeters (mm)

Package comparisons

Package data	SOT-23 (5-pin) TI – DBV	SC-70 (5-pin) TI – DCK	SOP (6-pin) TI – DRL	NanoStar™ package (5-/6-ball) TI – YZP	NanoStar package (4-ball) TI – YFP	NanoStar package (4-ball) TI – YZV
Length (mm)	2,90 ± 0,10	2,00 ± 0,15	1,60 ± 0,05	1,40 ± 0,05	0,82 + or - 0.05	0,90 ± 0,05
Width (mm)	2,80 ± 0,20	2,10 ± 0,30	1,60 ± 0,05	0,90 ± 0,05	0,82 + or - 0.05	0,90 ± 0,05
Height max (mm)	1,45	1,10	0,60	0,50	0,50	0,50
Footprint area (mm^2)	8,12	4,20	2,56	1,26	0,58	0,81

Dual-/triple-gate comparisons

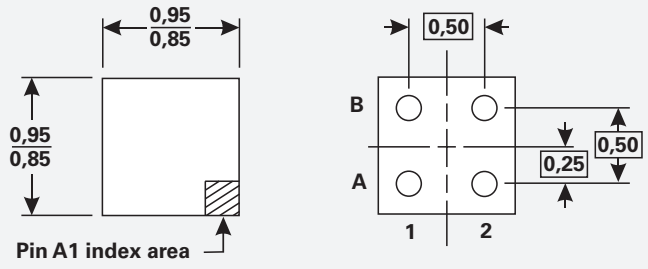
Package data	SOT-23 (6-pin) TI – DBV	SC-70 (6-pin) TI – DCK	SOP (6-pin) TI – DRL	SSOP (8-pin) TI – DCT	VSSOP (8-pin) TI – DCU	NanoStar package (8-ball) TI – YZP
Length (mm)	2,90 ± 0,10	2,00 ± 0,15	1,60 ± 0,10	2,95 ± 0,20	2,0 ± 0,10	1,90 ± 0,05
Width (mm)	2,80 ± 0,20	2,10 ± 0,30	1,60 ± 0,10	4,0 ± 0,25	3,10 ± 0,10	0,90 ± 0,05
Height (mm)	1,20 ± 0,25	0,95 ± 0,15	0,60	1,30 max	0,90 max	0,50 max
Footprint area (mm^2)	8,12	4,20	2,56	11,80	6,20	1,71

Package Data (continued)

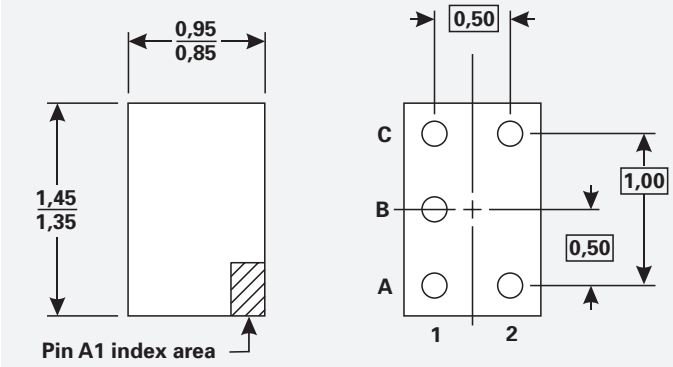
Package attributes

Attribute	4-ball	5-ball	6-ball	8-ball
Ball pitch (mm)	0,5	0,5	0,5	0,5
Ball diameter (mm)	0,23	0,23	0,23	0,23
Package length (mm)	0,9	1,4	1,4	1,9
Package width (mm)	0,9	0,9	0,9	0,9
Package height (mm)	0,5 max	0,5 max	0,5 max	0,5 max
Ball matrix (rows, columns)	2 x 2	3 x 2, depopulate 1	3 x 2	4 x 2
Ball metallurgy	Pb-free	Pb-free	Pb-free	Pb-free
Moisture level	Level 1 @ 260°C	Level 1 @ 260°C	Level 1 @ 260°C	Level 1 @ 260°C

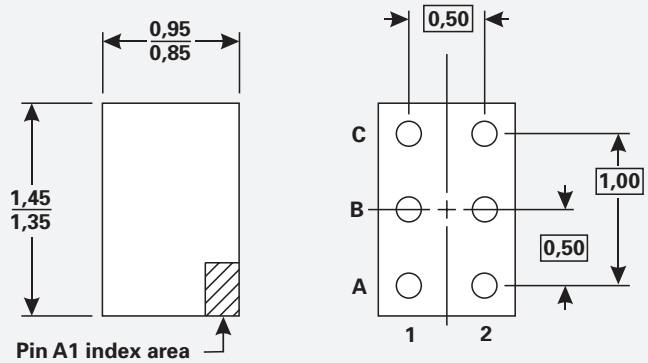
4-ball package



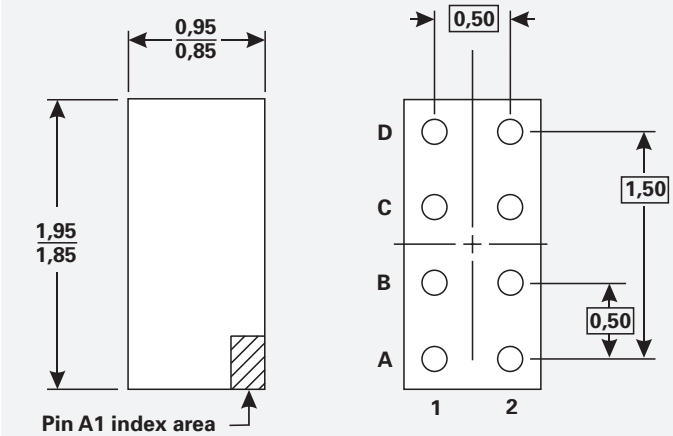
5-ball package



6-ball package

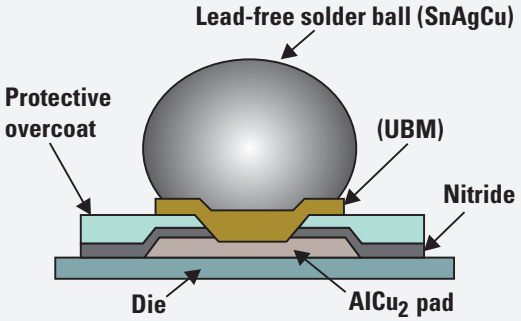


8-ball package

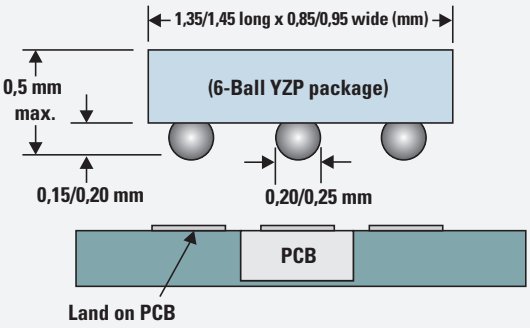


PBC Design Guidelines

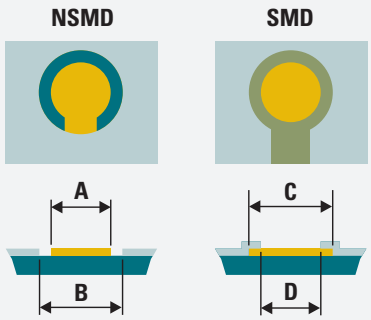
Solder ball composition



Package area configuration (0,5-mm ball pitch)



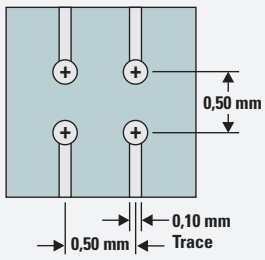
PCB design



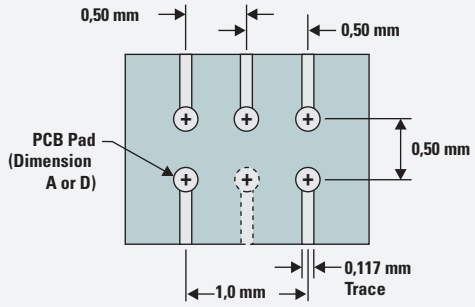
(YZP)

Non-solder mask defined (NSMD) preferred method		Solder mask defined (SMD)	
Copper pad	Solder mask opening	Copper pad	Solder mask opening
"A"	"B"	"C"	"D"
0,225 mm ± 0,025 mm	0,350 mm ± 0,025 mm	0,350 mm ± 0,025 mm	0,225 mm ± 0,025 mm

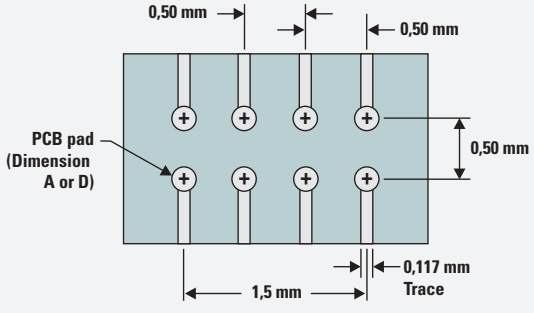
YZV 4-ball PCB pattern



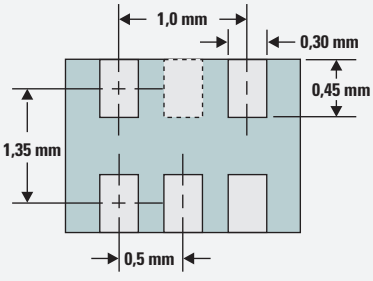
YZP 5-/6-ball PCB pattern



YZP 8-ball PCB pattern



DRL 5-/6-pin PCB pattern



Note:Trace width shall be ≤ two-thirds pad diameter.

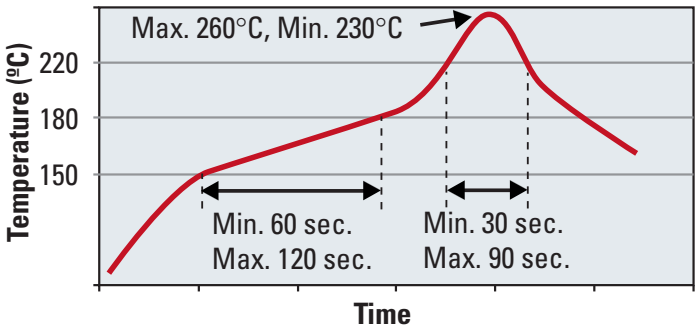
IR Reflow Profile

Dual-/triple-gate comparisons

	Pb	Pb-free
Ramp rate	3°C/sec. max.	3°C/sec. max.
Preheat	135°C to 165°C 60 to 120 sec.	150°C to 180°C 60 to 120 sec.
Time above liquidus	183°C 30 to 90 sec.	220°C 30 to 90 sec.
Peak Temp.	235°C ±5°C	255°C ±5°C
Time within 5°C peak temp.	20 to 40 sec.	20 to 40 sec.
Ramp down rate	6°C/sec. max.	6°C/sec. max.

Note: These are ideal profiles, and actual conditions obtained in any specified reflow oven will vary. The profiles are based on convection or RF plus forced convection heating.

Pb-free ball NanoStar integrated circuit package recommended temperature profile



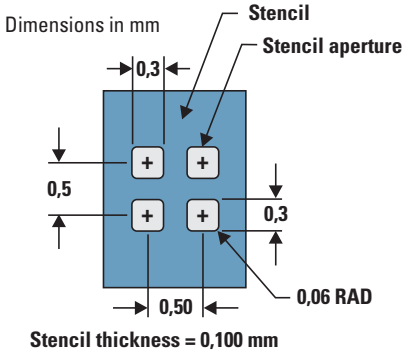
Stencil Vitals

Solder paste

TI recommends the use of type 3 or finer solder paste when mounting the WCSP. The use of paste offers the following advantages:

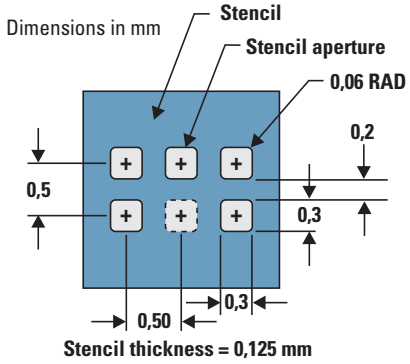
- Paste aids wetting of the solder ball to the PCB land.
- The adhesive properties of the paste will hold the component in place during reflow.
- Paste contributes to the final volume of solder in the joint, and thus allows this volume to be varied to give an optimum joint.
- Paste selection is normally driven by overall system assembly requirements. In general, the “no clean” compositions are preferred due to the difficulty in cleaning under the mounted components.

4-ball solder stencil



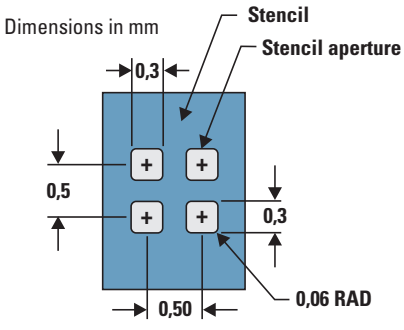
Stencil thickness = 0,100 mm

5-/6-ball solder stencil



Stencil thickness = 0,125 mm

8-ball solder stencil



Stencil thickness = 0,100 mm

Thermal Characteristics

Thermal impedance values at various airflow rates (model data per JESD 51-7 and JESD 51-3)

Package		Thermal impedance	Airflow (linear ft/minute)			
			0	150	250	500
4-ball	1S0P	$R_{\theta JA}$ (°C/W)	197.65	168.47	153.41	137.09
	1S2P	$R_{\theta JA}$ (°C/W)	120.62	114.25	106.9	99.9
	1S0P	$R_{\theta JA}$ (°C/W)	28.18	–	–	–
5-ball	1S2P	$R_{\theta JA}$ (°C/W)	131.56	129.26	128	126.08
		$R_{\theta JA}$ (°C/W)	18.0	–	–	–
6-ball	1S2P	$R_{\theta JA}$ (°C/W)	123.36	121.03	119.8	119.3
		$R_{\theta JA}$ (°C/W)	17.6	–	–	–
8-ball	1S2P	$R_{\theta JA}$ (°C/W)	101.92	99.69	98.5	96.75
		$R_{\theta JA}$ (°C/W)	13.79	–	–	–

Board-Level Reliability Data

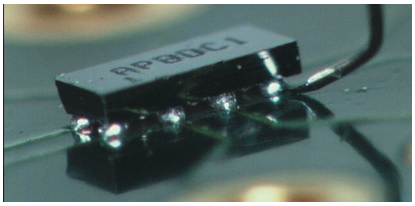
Board-Level Reliability N_1 (cycles to first failure)	
NanoStar™ (YZP)	>1,000 cycles

No underfill or adhesive was used, nor are these substances required for these packages.

Test parameters:
2 cycles/hr: –40°C to +125°C
0.8-mm thick FR4 epoxy board per IPC-9701, TC3, NTC-C

WCSP Testability

Solder Balls Provide Easy Access
Given the ideal placement of the solder balls along the outside of the package, along with sufficient ball height, probe tips can easily create a dedicated contact to individual pins.



Board-Mounting Pick-Up Tools

Because of the package size and configuration, we recommend a rectangular or circular shaped pick-up tool. We also recommend the tool have an outside diameter smaller than the package body, with a compliant tip. Recommended placement force is 125-200 gF.

Electrical Characteristics

WCSP (YZP)

	R (Ω)	L (nH)	C (pF)			
			4-ball	5-ball	6-ball	8-ball
Mean	0.001	0.021	0.046	0.046	0.046	0.043

Note: Electrical package parasitic was achieved through electrical modeling and is based on a 3-D model. Actual electrical data may differ slightly from simulated results.

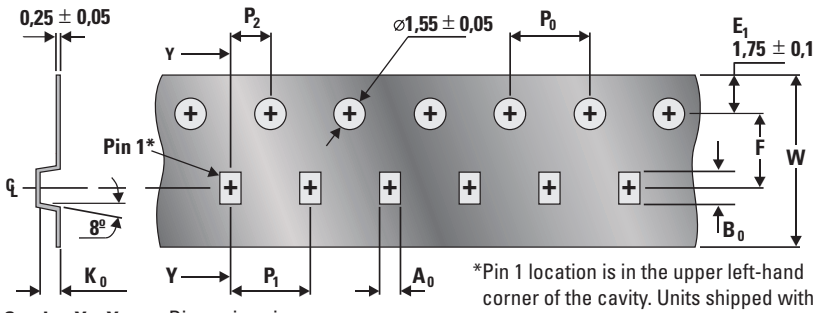
Little Logic product portfolio electrical performance

Family	Operating voltage range (V)	Optimized voltage (V)	Propagation delay (typ) (V)	Output drive (mA)	Input tolerance (V)	IOFF protection
AUC	0.8 to 2.7	1.8	2.0	8	3.6	Yes
AUP	0.8 to 3.6	3.3	3.0	4	3.6	Yes
LVC	1.65 to 5.5	3.3	3.0	24	5.5	Yes
AHC	2.0 to 5.5	5	5.0	8	5.5	No
AHCT	4.5 to 5.5	5	5.0	8	5.5	No
CBT	4.5 to 5.5	5	0.25*	–**	5.5	Yes
CBTD	4.5 to 5.5	5	0.25*	–**	5.5	Yes
CBTLV	2.3 to 3.6	3.3	0.25*	–**	3.6	Yes
CB3T	2.5 to 3.6	3.3	0.25*	–**	5.5	Yes

**The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance). The value listed is a maximum.*
***The FET switch has no output drive. The drive current at the output terminal is determined by the drive current of the device connected at the input terminal of the FET switch.*

Packaging Tape and Reel

Reel tape configuration



Section Y – Y

Dimensions in mm

*Pin 1 location is in the upper left-hand corner of the cavity. Units shipped with balls down.

Dimensions	4-ball	5 and 6-ball	8-ball
Pocket width, A0 (mm)	1,02 ± 0,05	1,02 ± 0,05	1,02 ± 0,05
Pocket length, B0 (mm)	1,02 ± 0,05	1,52 ± 0,05	2,02 ± 0,05
Pocket depth, K0 (mm)	0,63 ± 0,05	0,63 ± 0,05	0,63 ± 0,05
Pocket pitch, P1 (mm)	4,0 ± 0,1	4,0 ± 0,1	4,0 ± 0,1
Sprocket hole-to-pocket centerline, F (mm)	3,50 ± 0,05	3,50 ± 0,05	3,50 ± 0,05
Sprocket hole-to-pocket offset, P2 (mm)	2,0 ± 0,05	2,0 ± 0,05	2,0 ± 0,05
Sprocket hole pitch, P0 (mm)	4,00 ± 0,1	4,00 ± 0,1	4,00 ± 0,1
Tape width, W (mm)	8,00 ± 0,1	8,00 ± 0,3	8,00 ± 0,3
Reel diameter (mm) max.	178	178	178

Rework Procedure

There are several rework equipment vendors in the market offering well-designed equipment and established processes. Air-Vac Engineering (www.air-vac-eng.com) has established NanoStar™ package reflow profiles for both convection and contact heat (conduction) rework processes. A typical process for the convection using DRS-24NC equipment for a 0.056-inch thick FR4 board can be:

Eutectic balls

1) Apply flux to component using Auto Flux feature of DRS24.
2) Align device over pads.
3) Place device on board.
4) Raise nozzle .050”.
5) Preheat board to 90°C, nozzle warming up 20 percent air flow, 100°C.
6) Soak stage–20 percent air flow, 200°C, 90 seconds.
7) Ramp stage–20 percent air flow, 300°C, 30 seconds.
8) Reflow stage–25 percent air flow, 325°C, 55 seconds.
9) Cooldown stage–40 percent air flow, 25°C, 30 seconds.

Solder paste

1) Align device over pads.
2) Place device on board.
3) Raise nozzle .050”.
4) Preheat board to 90°C, nozzle warming up 20 percent air flow, 125°C.
5) Soak stage–20 percent air flow, 225°C, 90 seconds.
6) Ramp stage–20 percent air flow, 335°C, 30 seconds.
7) Reflow stage–25 percent air flow, 370°C, 65 seconds.
8) Cooldown stage–40 percent air flow, 25°C, 50 seconds.

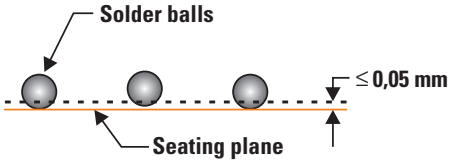
The recommended tooling for both the convection and conduction processes is:

Process	Nozzle description	Nozzle part number	Tray
Hot gas	NanoStar™ .0365” x .0560” x .0155” 5-ball	N09DVG-7	A04DVG06
Contact	NanoStar .0365” x .0560” x .0155” 5-ball	CE037-056TI	A0201X8-0X

Geometric Dimensional Tolerances

Coplanarity

This package meets a coplanarity of 0,05 mm as shown. Coplanarity is defined as a unilateral tolerance zone measured upward from the seating plane. (Reference ASME Y14.5M - 1994)



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